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APPLICATION

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TITLE: P-TYPE RESET/READOUT CIRCUITRY WITH N-TYPE PHOTODIODE FOR RADIATION HARD APS

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P-TYPE RESET/READOUT CIRCUITRY WITH N-TYPE PHOTODIODE FOR RADIATION HARD APS

CROSS REFERENCE TO RELATED APPLICATION

This application claims the benefit of the priority of U.S. Provisional Application No. 60/151,219, filed on August 26, 1999, and entitled P-Type Reset/Readout Circuitry for Radiation Hard APS.

BACKGROUND

The present disclosure generally relates to solid-state image sensors, and more specifically, to radiation hard active pixel sensors.

Charge coupled devices (CCD) have been used to process electronic image data. However, recent trend toward lower power consumption and greater system integration have spurred efforts to utilize existing sub-micron CMOS technology for electronic imaging applications.

Active pixel sensors (APS) are solid-state imagers where each pixel contains a photo-sensor, a photon to voltage converter, and a reset transistor. The APS detects image signals through a transistor switching rather than charge coupling. However, solid-state imagers may require a

protective enclosure in order to operate under radiation or space environment.

SUMMARY

In recognition of the above-described difficulties, the inventor recognized the need for providing a compact, radiation-hard active pixel sensor. Thus, the present disclosure discloses a pixel sensor that provides image sensing under radiation or space environment.

The pixel sensor includes a readout circuit and a first reset circuit. The readout circuit converts optical image signals to electronic signals, and includes p-type transistors and an n-type photosensitive element. The first reset circuit is configured to provide a reset level for a pixel output, and also includes p-type transistors. The use of p-type transistors and n-type photosensitive element provides radiation hardness without any radiation protective enclosure.

The present disclosure further includes a CMOS image sensor system, which includes an array of active pixel sensors, a control circuit, and a column readout circuit. Each pixel sensor of the array includes a pixel readout circuit and a first reset circuit. The pixel readout circuit converts optical image signals to electronic

signals, and includes p-type transistors and an n-type photosensitive element. The first reset circuit is configured to provide a reset level for a pixel output, and also includes p-type transistors. The control circuit provides timing and control signals to enable read out of data stored in the array of active pixel sensors. The column readout circuit receives and processes the data stored in the array of active pixel sensors.

BRIEF DESCRIPTION OF THE DRAWINGS

Different aspects of the disclosure will be described in reference to the accompanying drawings wherein:

FIG. 1 illustrates a conventional active pixel sensor and its associated readout circuitry;

FIG. 2 illustrates an embodiment of the present system configured to provide compact, radiation-hard active pixel sensor;

FIG. 3 shows a cross-section view of the pixel sensor;

FIG. 4 shows a simulation result with an active pixel sensor design;

FIG. 5 shows one implementation of a layout design using p-channel transistors and a square or a rectangular n-type photodiode;

FIG. 6 shows one implementation of a layout design using p-channel transistors and a circular photodiode;

FIG. 7 shows a pixel array having a mixture of p-channel transistors and an n-type photodiode;

FIG. 8A illustrates one embodiment of a typical size of a pixel sensor in accordance with the present system;

FIGS. 8B and 8C show minimum sizes of conventional pixel sensors, one having a square photodiode and another having a rectangular photodiode; and

FIG. 9 shows an embodiment of a CMOS image sensor system having pixels with n-type photodiodes and p-type transistors.

DETAILED DESCRIPTION

A conventional active pixel sensor and its associated readout circuitry are illustrated in FIG. 1. Each pixel 100 of the active pixel sensor may include a photosensitive element 102 buffered by a source-follower transistor 104 and a row selection switch, which can be implemented by a transistor 106. A signal "ROW" is applied to the gate of the row selection transistor 106 to enable a particular row of pixels. In some embodiments, the element 102 includes a photogate with a floating diffusion output separated by a transfer gate. In other embodiments, the photosensitive

element 102 includes a photodiode. Each pixel 100 also includes a reset switch that can be implemented as a transistor 108 controlled by a signal "RST" applied to its gate.

FIG. 1 further includes a column readout circuit 110 and an output stage 112. The column readout circuit 110 may include sample and hold circuits to sample both the reset and signal levels to reduce reset noise associated with the pixel as well as noise associated with the source-follower transistor 104. Multiple column readout circuits 110 are coupled to the output stage 112, which may include switched integrators. The output of the output stage 112 may be coupled to a source-follower transistor 114 and a load transistor 116. The illustrated conventional design of the active pixel sensor is often implemented with n-channel MOSFET transistors and a p-type photodiode as a photosensitive element 102. However, the above-described active pixel sensor design often requires a protective enclosure to operate under radiation or space environment.

The inventor recognized that p-channel MOSFET transistors provide significantly better protection against radiation than n-channel MOSFET transistors. A p-channel MOSFET transistor design also uses smaller silicon area. Further, a need for a protective enclosure may not be necessary with p-channel transistor design. However,

traditional p-type photodiodes often suffer from low quantum efficiency. The quantum efficiency provides a measure of conversion efficiency between photons picked up by a photosensitive element and a number of electrons converted from the photons. Further, possible latch-up problems, when reset level exceeds V_{DD} due to the charge injection of a switch, caused the prior designs to prefer n-channel transistors.

FIG. 2 illustrates an embodiment of the present system 200 configured to provide a compact, radiation-hard active pixel sensor. The system also produces a large output signal range that may be important for individual pixel reset application. In the illustrated embodiment, the active pixel sensor and its associated readout circuitry are implemented with p-channel transistors and an n-type photodiode as a photosensitive element 204. In one embodiment, the transistors are MOSFET transistors.

The p-channel MOSFET transistor design may provide radiation hardness without the need for a protective enclosure. In addition, the n-type photodiode provides better quantum efficiency than p-type photodiodes. Further, as illustrated in FIG. 3, the n-type photodiode configuration allows formation of p+ guard rings connected to the ground around the n-type photodiode. The grounded

guard rings may substantially reduce leakage current and prevent any latch-ups.

In the illustrated embodiment of FIG. 2, each pixel 202 of the active pixel sensor 200 may include an n-type photo-sensitive element 204 buffered by a p-channel MOSFET source-follower transistor 206 and a row selection switch which can be implemented by a p-channel MOSFET transistor 208. A signal "ROW" is applied to the gate of the row selection transistor 208 to enable a particular row of pixels. Each pixel 202 also includes a reset switch that can be implemented as a p-channel MOSFET transistor 210 controlled by a signal "RST" applied to its gate. An optional p-channel reset transistor 212 is provided for individual pixel reset application. This reset transistor 212 may allow a pixel-by-pixel reset operation instead of the row-by-row operation.

When R_{RST} is at logic low and C_{RST} at logic high, the reset switch 210 is turned off. However, the n-type well 306 (see FIG. 3) connected to V_{DD} allows the leakage current of a small photodiode (drain of the reset transistor) to charge the node 214 higher while the leakage current of an n-type reset transistor discharges the node 214 lower as the n-type photodiode. Thus, the p-channel transistors provide smaller leakage current than the n-channel transistors.

However, when R_{RST} is at logic low and C_{RST} at logic low, the reset switch 210 may be turned on by a p-channel threshold voltage (V_{thp}) at the gate of the reset switch 210. The above-described configuration resets the node 214 to V_{RST}, which is equal to V_{DD} minus a small voltage of about 0.7 volts (V_{thp}). This reset voltage (V_{RST}) further prevents any latch-up problems caused by a reset level exceeding V_{DD} due to the charge injection of the reset switch.

The reset voltage (V_{RST}) needs to stay below the supply voltage (V_{DD}) to keep the p-channel source follower transistor 206 in the linear region. By keeping the source follower 206 in the linear region, the active pixel sensor has hard reset levels such as small fixed pattern noise and uniform reset levels.

The p-channel transistor design of the active pixel sensor 200 also includes p-channel load transistors 216, 218 and a p-channel output source-follower 220.

Referring to FIG. 3, the n-type photodiode 300 is guarded by a pair of p+ guard rings 302 connected to the ground. The photodiode 300 and the guard rings 302 are provided over a p-type substrate 304. N-type wells 306 on either side are connected to V_{DD}. The wells 306 are configured to prevent crosstalk between pixels.

A simulation result with an active pixel sensor design as described above is shown in FIG. 4. The result shows

that when a row is selected, the output follows the voltage level of PIX node 214. When C_{RST} (along with R_{RST}) is set to logic low, PIX node 214 is reset to V_{RST}. Thus, the active pixel sensor of the present system provides large output swing and hard reset level. As a result, the dynamic range of the sensor increases.

FIGS. 5 through 7 illustrate different layout implementations of the active pixel sensor using the design described above. FIG. 5 shows one implementation of a layout design using p-channel transistors and a square or a rectangular n-type photodiode. FIG. 6 shows one implementation of a layout design using p-channel transistors and a circular photodiode. FIG. 7 shows a pixel array having a mixture of above-described pixel designs. This pixel array may be used in an active pixel sensor design to provide image sensing under radiation environment.

FIGS. 8A to 8C show comparison of areal density between the p-channel transistor/ n-type photodiode design and conventional n-channel transistor designs.

FIG. 8A illustrates one embodiment of a typical size of a pixel sensor in accordance with the present system. The pixel sensor has an n-channel square photodiode. The minimum size of this pixel sensor is measured to be approximately $(14\ \mu m)^2$.

FIGS. 8B and 8C show minimum sizes of conventional pixel sensors, one having a square photodiode and another having a rectangular photodiode. The rectangular photodiode design requires minimum size of approximately $(21\ \mu m)^2$ while the square photodiode requires minimum size of approximately $(28\ \mu m)^2$. Thus, it is shown that pixel sensor design of the present system requires less than half the size of the conventional design. Further, the conventional design would also require a bulky enclosure to protect the pixel array from the radiation.

FIG. 9 shows an embodiment of a CMOS image sensor system 900. The system includes an array of active pixel sensors 902 and a controller 904. Each active pixel sensor may be implemented with p-channel MOSFET transistors and an n-type photodiode. The controller 904 provides timing and control signals to enable read out of signals stored in the pixels.

The image array 902 data is read out a row at a time using column-parallel readout architecture, as illustrated by a column readout circuit 110 in FIG. 1. The controller 904 selects a particular row of pixels in the array 902 by controlling the operation of the vertical addressing circuit 906 and row drivers 908. Charge signals stored in the selected row of pixels are provided to a readout circuit

910. The pixels read from each of the columns can be read out sequentially using a horizontal addressing circuit 914. The output of the readout circuit 910 is directed to an output stage buffer 912. The output stage buffer 912 includes a p-type source-follower MOSFET transistor similar to the source-follower 220, and a p-type load transistor 218 as shown in FIG. 2.

While specific embodiments of the invention have been illustrated and described, other embodiments and variations are possible. For example, although the transistors used in the pixel sensors have been described in terms of MOSFET transistors, other types of transistors, such as JFET or bipolar transistors, may be used in the pixel sensors.

All these are intended to be encompassed by the following claims.